DCSG S9501 Series
CPLD Specification

R 1.0

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UfiSpace Technology Corporation

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Revision History

Date	Rev	Author	Summary of Change
Jun. 8, 2021	R1.0	Hector Zhang	First Draft Release

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1 Overview

By providing 1GE, 2.5GE, 10GE high speed Ethernet ports and IEEE 1588v2, SyncE timing synchronization features, S9501 Series enables service providers to migrate 2G, 3G, 4G BBUs to 5G RAN to firm NSA network, it's also suitable for 5G SA RAN network connection when only 1G/10G ports are necessary.

With temperature-hardened, high port density, high-throughput, small form factor, low-power-consumption & redundancy (PSU and FAN) features, S9501 Series delivers high timing synchronization precision, ultra-low latency, temperature harden and high system reliability, excellent Ethernet switching performance and intelligence to the mobile/radio access network edge in a compact 1RU form factor that helps reduce infrastructure and administrative costs.

S9501 Series SKUs, I/O ports, PSU and FAN configurations are shown as below:

SKU	1G/2.5G/10G Ethernet Ports	FAN	PSU	Timing
S9501-28SMT	4-port 100M/GE RJ45 16-port 100M/GE/2.5G SFP 6-port GE/2.5G/10GE SFP+ 2-port GE/10GE SFP+ w/ MACSec	2+1 Redundant fan FRU	1+1 Redundant 200W PSU FRU AC or DC options	GNSS, ToD, 1PPS, 10M In or Out, T1/E1 Input
S9501-18SMT	4-port 100M/GE RJ45 8-port 100M/GE/2.5G SFP 6-port GE/2.5G/10GE SFP+	2+1 Redundant fab FRU	1+1 Redundant 200W PSU FRU AC or DC options	GNSS, ToD, 1PPS, 10M In or Out

Table 1-1 S9501 Series Configuration Information

S9501 Series models' front panel and rear panel design are shown as below:



Figure 1-1 ID Rendering -- S9501-28SMT Front Panel



Figure 1-2 ID Rendering -- S9501-18SMT Front Panel



Figure 1-3 ID Rendering – Rear Panel (Same for all models)

2 High-Level Description

This section describes key features, system block diagram and system mechanical outline for S9501 Series.

2.1 Feature Summary

- Ethernet I/O ports:

  S9501-28SMT:
  - 4 x 100M/1GE RJ45 ports
  - 16 x 100M/1G/2.5GE SFP ports
  - 6 x 1G/2.5G/10GE SFP+ ports
  - 2 x 1G/10GE SFP+ ports with MACSec option

  S9501-18SMT:
  - 4 x 100M/1GE RJ45 ports
  - 8 x 100M/1G/2.5GE SFP ports
  - 6 x 1G/2.5G/10GE SFP+ ports
- Front/Real panel LED indicators:
  - 1 x power status LED
  - 1 x fan status LED
  - 1 x system status LED
  - 1 x synchronization status LED
  - 1 x GNSS\GPS status LED
  - Per port FAN status LED
  - Per port PSU status LED
  - Per port link status LED
- Management interfaces:
  - 1 x GE OOB management port (CPU/BMC)
  - 1 x USB2.0 Type-A general purpose port
  - 1 x RS232 console port in RJ45 form factor
  - 1 x tact switch for system reset/reload default configuration
- Timing Synchronization:
  - 1588V2 and SyncE with T-GM, T-TC, T-BC support
  - Input source : GNSS, E1/T1 **(S9501-28SMT only)**, ToD(RJ45), 1PPS(SMB) and 10MHz(SMB)
  - Output source : ToD(RJ45), 1PPS(SMB) and 10MHz(SMB)

2.2 Component Summary

- PCBA:
  - 1 x Switch board (BOM option will be vary based on SKU definition)

- 1 x CPU card
- 1 x FAN card
- 1 x NTM card
- 1 x BMC card
- 1 x PSU card

- On board key components:
  - Switch Board
    - 1 x Q-UX MAC:
      - ✓ **S9501-28SMT:** BCM88270,
      - ✓ **S9501-18SMT:** BCM88272,
    - 2 x 512MB DDR4 SDRAM @ 800MHz
    - 1 x Dual port 10GbE PHY BCM82759 (**S9501-28SMT only)**
    - 1 x Quad port 1GbE PHY BCM54140
    - 1 x management CPLD 10M04SAU324I7G
    - 1 x PCIe/NCSI NIC I210-IT for CPU & BMC
    - 1 x Clock jitter attenuator buffer Si5344D
    - 1 x Clock Generator ZL30262LDG1
    - 1 x GNSS module NEO-M8T
    - 1 x T1/E1 transceiver 82P2281 (**S9501-28SMT only)**
    - 1 x 32GB M.2 SSD memory module
  - CPU Card
    - 1 x CPU Denverton-NS C3508 with two/four cores @ 1.6GHz
    - 1 x 8GB DDR4 SODIMM memory module with ECC support
- PSU Card:
  - 2x 200W slim PSUs with redundancy support
- FAN Card:
  - 3x FAN tray modules with 2+1 redundancy support
- Timing Card:
  - 1x DPLL ZL30773 or ZL30795
  - 1x FPGA M2GL005VFG256I
- BMC Card:

1x AST2600A1 or AST2620A2

3 Main Board

3.1 Features Summary and Diagram

Main functional blocks in the system CPLD include the following:

- Model ID and Revision information
- Component reset control
- interrupt management
- I2C / USB / UART bus select control
- Front panel & FAN board LED control
- ROV control
- Watch Dog function for CPU and BMC

Two interfaces connected between CPU and CPLD: I2C bus and LPC bus.

CPU can access CPLD by I2C bus channel 0 and address is 7b'0110011x (H33). LPC interface will be active to access CPLD when LPC address 07

CPLD function diagram is as below:

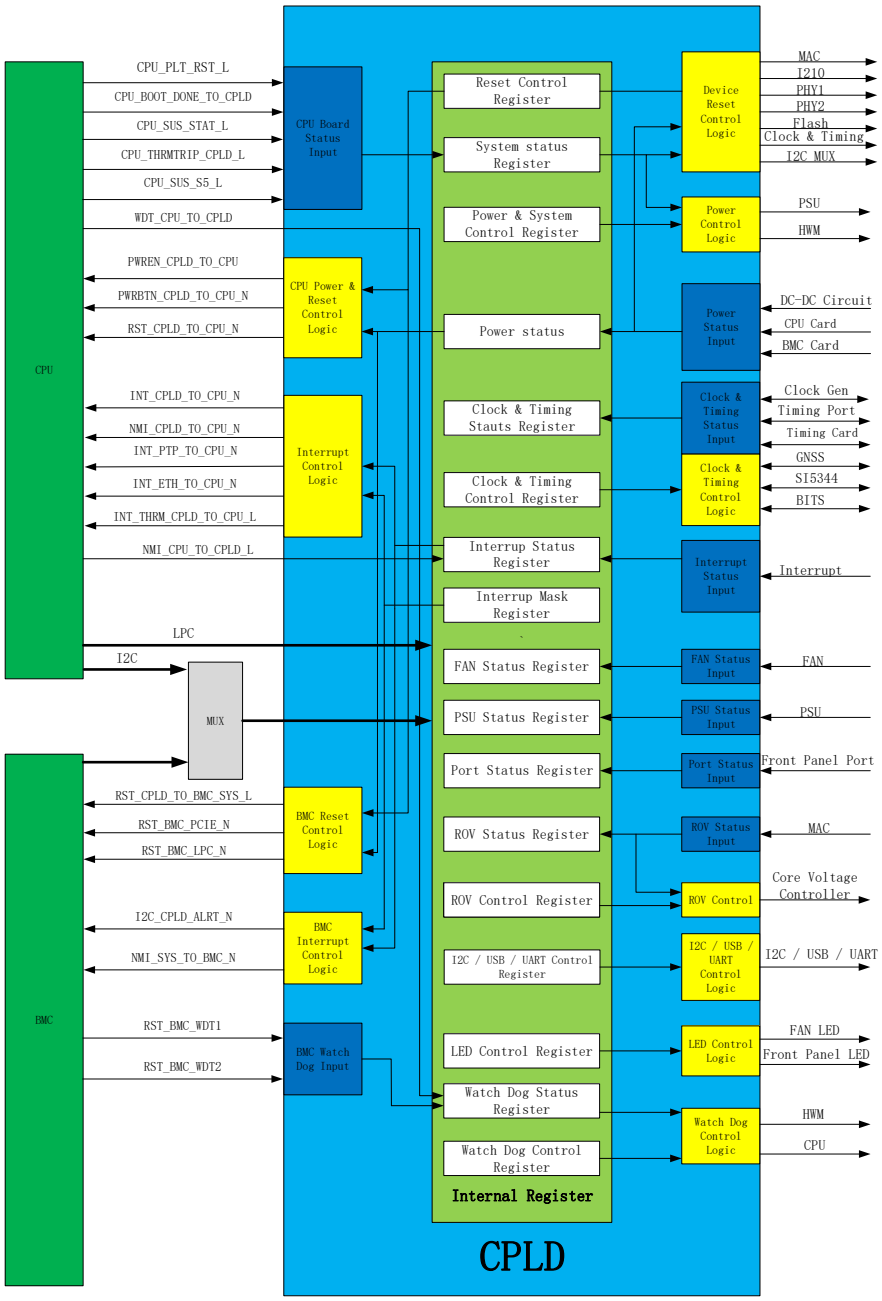


Figure 3-1 CPLD diagram

3.2 *MB CPLD Pin Assignment*

Switch board CPLD pin assignment is shown as below:

Number	Name	Net Name	Pin Description
R16	IO_5/DIFFIO_RX_R2N	BIOS_BOOT_SEL0	BIOS boot select
R17	IO_5/DIFFIO_RX_R9N	BIOS_BOOT_SEL1	BIOS boot select
V14	IO_4/DIFFIO_RX_B22P	BMC_PRSNT_L	BMC present
U15	IO_4/DIFFIO_RX_B26P	BMC_SGPMCK	SGPMIO
U16	IO_4/DIFFIO_TX_RX_B27N	BMC_SGPMI	SGPMIO
U13	IO_4/DIFFIO_RX_B19P	BMC_SGPMLD	SGPMIO

Number	Name	Net Name	Pin Description
U12	IO_4/DIFFIO_RX_B19N	BMC_SGPMO	SGPMIO
A2	IO_8/DIFFIO_RX_T27P	BMC_USB_MUX_SEL	BMC USB MUX select
V13	IO_4/DIFFIO_RX_B22N	CLK_25M_CPLD	25Mhz clock input from oscillator
M3	IO_2/CLK0P/DIFFIO_RX_L18P	CLK_25M_CPLD_CLK0	25Mhz clock input from DPLL
T7	IO_3/DIFFIO_RX_B8N	CLK_33M_LPC_CPLD	LPC 33Mhz clock
H1	IO_1B/DIFFIO_RX_L10P	CPLD_BUILD_ID0	CPLD build ID 0
J4	IO_1B	CPLD_BUILD_ID1	CPLD build ID 1
J6	IO_1B/DIFFIO_RX_L14N	CPLD_HW_REV_ID0	CPLD hardware revision ID 0
K7	IO_1B/DIFFIO_RX_L14P	CPLD_HW_REV_ID1	CPLD hardware revision ID 1
F5	IO_1A/ADC1IN5/DIFFIO_RX_L5N	CPLD_REV_ID0	CPLD revision ID 0
D1	IO_1A/ADC1IN13/DIFFIO_RX_L6N	CPLD_REV_ID1	CPLD revision ID 1
E5	IO_1A/ADC1IN6/DIFFIO_RX_L5P	CPLD_REV_ID2	CPLD revision ID 2
U3	IO_3/DIFFIO_RX_B2N	CPLD_SKU_ID0	CPLD SKU ID 0
T4	IO_3/DIFFIO_TX_RX_B1P	CPLD_SKU_ID1	CPLD SKU ID 1
V2	IO_3/DIFFIO_RX_B2P	CPLD_SKU_ID2	CPLD SKU ID 2
P6	IO_3/DIFFIO_TX_RX_B3N	CPLD_SKU_ID3	CPLD SKU ID 3
J12	IO_6/DIFFIO_RX_R20N	CPU_BATLOW_L	CPU baterry voltage low
P16	IO_5	CPU_BOOT_DONE_TO_CPLD	CPU booting done
V5	IO_3/DIFFIO_RX_B6P	CPU_PLT_RST_L	CPU platform reset
V17	IO_4/DIFFIO_RX_B28P	CPU_PWRGD_TO_CPLD	CPU power good
T18	IO_5/DIFFIO_RX_R4N	CPU_SUS_S5_L	CPU S5 state
T17	IO_5/DIFFIO_RX_R9P	CPU_SUS_STAT_L	CPU STAT state
V16	IO_4/DIFFIO_RX_B28N	CPU_THRMTRIP_CPLD_L	CPU thermaltrip
E2	ANAIN1	GND	Unused
L3	IO_2/CLK0N/DIFFIO_RX_L18N	GND	Unused
K8	IO_2/CLK1N/DIFFIO_RX_L20N	GND	Unused
M4	IO_2/DPCLK0/DIFFIO_RX_L22N	GND	Unused
K12	IO_6/CLK2P/DIFFIO_RX_R14P	GND	Unused
L17	IO_6/CLK3P/DIFFIO_RX_R16P	GND	Unused
H11	IO_6/DPCLK3/DIFFIO_RX_R26P	GND	Unused
G10	IO_8/DIFFIO_RX_T14N	GNSS_ANT_ON	GNSS antennnae on
A10	IO_8/DIFFIO_RX_T13N	GNSS_ANT_OPEN	GNSS antennnae open

Number	Name	Net Name	Pin Description
K2	IO_1B/DIFFIO_RX_L15N	GNSS_ANT_PWREN	GNSS antennnae power enable
C1	IO_1A/ADC1IN12/DIFFIO_RX_L4P	GNSS_ANT_SHORT_N	GNSS antennnae short
V8	IO_3/DIFFIO_RX_B13P	HWM_FAN_PRSNT_N	FAN board present
U9	IO_3/DIFFIO_TX_RX_B12P	HWM_FAN2_PRSNT_N	FAN2 present
T9	IO_3/DIFFIO_TX_RX_B16N	HWM_FAN3_PRSNT_N	FAN3 present
V9	IO_3/DIFFIO_TX_RX_B12N	HWM_FAN4_PRSNT_N	FAN4 present
R18	IO_5/DIFFIO_RX_R12P	I2C_CPLD_ALRT_N	I2C alert to BMC
A9	IO_8/DIFFIO_RX_T15P	I2C_CPLD_MUX_EN	Switch CPLD I2C to CPU or BMC
A13	IO_7/DIFFIO_RX_T11P	I2C_CPLD_SCL	CPLD I2C
A11	IO_8/DIFFIO_RX_T13P	I2C_CPLD_SDA	CPLD I2C
E15	IO_6/PLL_R_CLKOUTP/DIFFIO_RX_R33P	I2C_HWM_CNTRL	Hardware monitor control
D14	IO_7/DIFFIO_RX_T1N	I2C_MANF_MUX_SEL	Switch MANF I2C to CPU or BMC
P10	IO_4/DIFFIO_TX_RX_B18N	I2C_NIC_ARLT_N	I210 I2C alert
M16	IO_5/DIFFIO_RX_R6N	I2C_VCORE_SCL	VCORE I2C
M15	IO_5/DIFFIO_RX_R5N	I2C_VCORE_SDA	VCORE I2C
T15	IO_4/DIFFIO_TX_RX_B25P	I2C0_HWM_MUX_SEL	Switch hardware monitor I2C to CPU or BMC
K11	IO_6/CLK2N/DIFFIO_RX_R14N	I2C0_PSU_MUX_SEL	Switch PSU I2C to CPU or BMC
C7	IO_8/DIFFIO_RX_T21N	INT_BITS_N	BIS interrupt
M11	IO_5/DIFFIO_RX_R3N	INT_CJA_INTR_N	SI5344 interrupt
M10	IO_4/DIFFIO_TX_RX_B20N	INT_CJA_LOL_N	SI5344 LOL interrupt
P14	IO_5/DIFFIO_RX_R1N	INT_CPLD_TO_CPU_N	I2C Alert to CPU
B9	IO_8/DIFFIO_RX_T16P	INT_DPLL_1588_L	DPLL 1588 interrupt
B4	IO_8/DIFFIO_RX_T23N	INT_DPLL_SYNC_L	DPLL 1588 interrupt
E17	IO_6/DIFFIO_RX_R30N	INT_ETH_TO_CPU_N	ETH interrupt
V10	IO_3/DIFFIO_RX_B15N	INT_FAN_CARD_N	FAN board interrupt
V4	IO_3/DIFFIO_RX_B4P	INT_FAN2_N	FAN2 interrupt
T8	IO_3/DIFFIO_RX_B8P	INT_FAN3_N	FAN3 interrupt
V7	IO_3/DIFFIO_RX_B11P	INT_FAN4_N	FAN4 interrupt
U18	IO_5/DIFFIO_RX_R4P	INT_HWM_ALERT_N	Hardware monitor alert
B12	IO_7/DIFFIO_RX_T9N	INT_HWM_NMI_N	Hardware monitor non maskable interrupt
P5	IO_3/DIFFIO_TX_RX_B3P	INT_INTRUDER_CPLD_N	intruder interrupt
N15	IO_5/DIFFIO_RX_R5P	INT_INTURDER_SW_N	intrude control
R10	IO_4/DIFFIO_TX_RX_B21N	INT_MAC_N	MAC interrupt
B7	IO_8/VREFB8N0	INT_NTM_L	Timing card interrupt
H2	IO_1B/DIFFIO_RX_L10N	INT_PHY1_N	PHY1 interrupt

Number	Name	Net Name	Pin Description
D17	IO_6/DIFFIO_RX_R34P	INT_PSU1_N	PSU1 interrupt
D16	IO_6/DIFFIO_RX_R29N	INT_PSU2_N	PSU2 interrupt
E18	IO_6	INT_PTP_TO_CPU_N	PTP interrupt to CPU
L8	IO_2/CLK1P/DIFFIO_RX_L20P	INT_SFP+_ABS_N0	IO expander for SFP/SFP+ present interrupt
T6	IO_3/DIFFIO_TX_RX_B7P	INT_SFP+_ABS_N1	IO expander for SFP/SFP+ present interrupt
J3	IO_1B/VREFB1N0	INT_SFP+_FLT_N0	IO expander for SFP/SFP+ TX fault interrupt
T5	IO_3/DIFFIO_TX_RX_B7N	INT_SFP+_FLT_N1	IO expander for SFP/SFP+ TX fault interrupt
R4	IO_3/DIFFIO_TX_RX_B1N	INT_SFP+_LOS_N0	IO expander for SFP/SFP+ RX lost interrupt
M2	IO_2/DIFFIO_RX_L19P	INT_SFP+_LOS_N1	IO expander for SFP/SFP+ RX lost interrupt
G18	IO_6/DIFFIO_RX_R18N	INT_THRM_CHIP_N	Thermaltrip interrupt
T16	IO_5/DIFFIO_RX_R2P	INT_THRM_CPLD_TO_CPU_L	Thermal interrupt to CPLD
L10	IO_4/DIFFIO_TX_RX_B20P	INT_TSEN_ALRT_N	Temperature sensor alert
B13	IO_7/DIFFIO_RX_T7N	INT_TSEN_NMI_N	Temperature sensor non maskable interrupt
U17	IO_4/DIFFIO_TX_RX_B27P	INT_VCORE_ALRT_N	VCORE alert
V15	IO_4/DIFFIO_RX_B26N	INT_VCORE_VR_FAULT_N	VCORE VR fault
E4	IO_1A/ADC1IN2/DIFFIO_RX_L1P	INT1_GNSS_N	GNSS interrupt
J8	IO_1B/TCK/DIFFIO_RX_L11P	JTAG_CPLD_TCK	JTAG
H3	IO_1B/TDI/DIFFIO_RX_L12N	JTAG_CPLD_TDI	JTAG
H4	IO_1B/TDO/DIFFIO_RX_L12P	JTAG_CPLD_TDO	JTAG
J7	IO_1B/TMS/DIFFIO_RX_L11N	JTAG_CPLD_TMS	JTAG
T10	IO_3/DIFFIO_TX_RX_B16P	LED_CPLD_STATUS1	CPLD LED
T11	IO_4/VREFB4N0	LED_CPLD_STATUS2	CPLD LED
T13	IO_4/DIFFIO_RX_B24N	LED_CPLD_STATUS3	CPLD LED
T14	IO_4/DIFFIO_RX_B24P	LED_CPLD_STATUS4	CPLD LED
G6	IO_1A/ADC1IN3/DIFFIO_RX_L3N	LED_ETH_STAT_CLR_N	Port LED clear
H6	IO_1A/ADC1IN4/DIFFIO_RX_L3P	LED_FAN_CLR_N	FAN board LED clear
U5	IO_3/DIFFIO_RX_B6N	LED_FAN_SCLK	FAN board LED serial clock signal
U6	IO_3/VREFB3N0	LED_FAN_SDAT	FAN board LED serial date signal
B1	IO_1A/ADC1IN11/DIFFIO_RX_L4N	LED_SYS_STAT_CLR_N	Front panel LED clear

Number	Name	Net Name	Pin Description
F1	IO_1A/ADC1IN15/DIFFIO_RX_L8N	LED_SYS_STAT_SCLK	Front panel LED serial clock signal
E1	IO_1A/ADC1IN14/DIFFIO_RX_L6P	LED_SYS_STAT_SDAT	Front panel LED serial date signal
T12	IO_4	LOCK_MAC_SYNCE_RCVD1	MAC SYNCE lock
C15	IO_7/DIFFIO_RX_T4N	LPC_FRAME_PCH_N	LPC
C18	IO_6/DIFFIO_RX_R32P	LPC_LAD0_PCH	LPC
B14	IO_7/DIFFIO_RX_T7P	LPC_LAD1_PCH	LPC
B18	IO_6/DIFFIO_RX_R32N	LPC_LAD2_PCH	LPC
A12	IO_7/DIFFIO_RX_T11N	LPC_LAD3_PCH	LPC
D18	IO_6/DIFFIO_RX_R30P	LPC_SERIRQ_CPLD_N	LPC
V11	IO_3/DIFFIO_RX_B15P	MAC_COREPLL_LOCK	MAC core PLL lock
V12	IO_3/DIFFIO_RX_B17N	MAC_MCUPLL_LOCK	MAC MCU PLL lock
L15	IO_5/DIFFIO_RX_R10P	MAC_VCORE_ROV0	MAC ROV 0
L16	IO_5/DIFFIO_RX_R11P	MAC_VCORE_ROV1	MAC ROV 1
N16	IO_5/DIFFIO_RX_R6P	MAC_VCORE_ROV2	MAC ROV 2
H7	IO_1B/JTAGEN/DIFFIO_RX_L9P	N20536139	Unused
H9	INPUT_ONLY_8/NCONFIG	N20536224	Unused
H8	IO_8/CONF_DONE/DIFFIO_RX_T24N	N20536226	Unused
G8	IO_8/NSTATUS/DIFFIO_RX_T24P	N20536228	Unused
E3	REFGND	N20537750	Unused
M17	IO_6/DIFFIO_RX_R15P	N28467037	Unused
L18	IO_6/DIFFIO_RX_R15N	N28467046	Unused
K18	IO_6/DIFFIO_RX_R17P	N28467055	Unused
J18	IO_6/DIFFIO_RX_R17N	N28467064	Unused
H18	IO_6/DIFFIO_RX_R18P	N28467073	Unused
H17	IO_6/DIFFIO_RX_R19P	N28467082	Unused
D4	IO_1A/ADC1IN1/DIFFIO_RX_L1N	NIC1_DEV_OFF_N	I210 disable
P15	IO_5/DIFFIO_RX_R7N	NMI_CPLD_TO_CPU_N	CPLD to CPU non maskable interrupt
C13	IO_7/DIFFIO_RX_T6N	NMI_CPU_TO_CPLD_L	CPU to CPLD non maskable interrupt
U8	IO_3/DIFFIO_RX_B13N	NMI_SYS_TO_BMC_N	CPLD to BMC non maskable interrupt
L2	IO_1B/DIFFIO_RX_L17P	NTM_PRSNT_L	Timing card present
C5	IO_8/DIFFIO_RX_T22P	P3V3_BMC_PG	BMC card P3V3_BMC power good
C11	IO_7/DIFFIO_RX_T10P	P3V3_EN_BROADSYNC	Enable timing card P3V3

Number	Name	Net Name	Pin Description
R5	IO_3/DIFFIO_TX_RX_B5N	PHY1_SYNCE_RCVD_LOCK	PHY1 SYNCE lock
U2	IO_2/DIFFIO_RX_L28P	PHY2_INT_N	PHY2 interrupt
N4	IO_2/PLL_L_CLKOUTN/DIFFIO_RX_L27N	PHY2_SERBOOT	PHY2 boot setting
B17	IO_7/DIFFIO_RX_T2P	PSU1_PRSNT_N	PSU1 present
A17	IO_7	PSU1_VIN_PWROK	PSU1 VIN power OK
C17	IO_6/DIFFIO_RX_R34N	PSU1_VOUT_PWROK	PSU1 VOUT power OK
B16	IO_7/DIFFIO_RX_T2N	PSU2_PRSNT_N	PSU2 present
A16	IO_7/VREFB7N0	PSU2_VIN_PWROK	PSU2 VIN power OK
C16	IO_7/DIFFIO_RX_T4P	PSU2_VOUT_PWROK	PSU2 VOUT power OK
A5	IO_8/DIFFIO_RX_T19N	PTP_10M_RS422_DIR_CNTRL	TOD port 10 Mhz in/out control
V3	IO_3/DIFFIO_RX_B4N	PTP_1PPS_BITS_MUX_SEL	Timing card BITS input select
A3	IO_8/DIFFIO_RX_T25P	PTP_1PPS_RS422_DIR_CNTRL	TOD port 1PPS in/out control
A6	IO_8/DIFFIO_RX_T19P	PTP_TOD_RS422_DIR_CNTRL	CP2105 UART/Timing card UART to TOD in/out control
A4	IO_8/DIFFIO_RX_T23P	PTP_UART_RS422_DIR_CNTRL	CPU UART to TOD in/out control
R11	IO_4/DIFFIO_TX_RX_B21P	PWRBTN_CPLD_TO_CPU_N	CPLD to CPU PWRBTN_N
D15	IO_6/PLL_R_CLKOUTN/DIFFIO_RX_R33N	PWREN_CPLD_TO_CPU	CPLD to TO_CPU PWROK
J15	IO_6/DIFFIO_RX_R22P	PWREN_SYS_DC_CPU_L	Enable main board main power
J16	IO_6/DIFFIO_RX_R23P	PWREN_SYS_P12V_CPU_L	Enable 12V
K4	IO_1B/DIFFIO_RX_L16N	PWRGD_BMC_TO_SYS	BMC card power good
R15	IO_5/DIFFIO_RX_R7P	PWROK_SYS_DC	main board power good
A7	IO_8	RST_BITS_N	BITS reset
J2	IO_1B/DIFFIO_RX_L13N	RST_BMC_LPC_N	BMC LPC reset
K15	IO_5/DIFFIO_RX_R10N	RST_BMC_PCIE_N	BMC PCIE reset
K3	IO_1B/DIFFIO_RX_L16P	RST_BMC_WDT1	BMC watch dog
E14	IO_7/DIFFIO_RX_T1P	RST_BMC_WDT2	BMC watch dog
H12	IO_6/DPCLK2/DIFFIO_RX_R26N	RST_BTN_FP_L	BTN reset to BMC
V6	IO_3	RST_CJA_N	SI5344 reset
R3	IO_2/DIFFIO_RX_L23N	RST_CLK_GEN_N	Clock generator reset
A8	IO_8/DIFFIO_RX_T15N	RST_CP2104_TOD_N	CP2105 reset
C6	IO_8/DIFFIO_RX_T20P	RST_CPLD_PWRUP_L	CPLD power up reset
A15	IO_7/DIFFIO_RX_T5P	RST_CPLD_TO_BMC_SYS_L	BMC system reset
K17	IO_6/CLK3N/DIFFIO_RX_R16N	RST_CPLD_TO_CPU_N	CPU system reset
K1	IO_1B/DIFFIO_RX_L15P	RST_GNSS_N	GNSS reset

Number	Name	Net Name	Pin Description
F11	IO_7/DIFFIO_RX_T8P	RST_I2C_MUX0_N	I2C MUX0 reset
L12	IO_5/DIFFIO_RX_R8P	RST_I2C_MUX2_N	I2C MUX2 reset
J1	IO_1B/DIFFIO_RX_L13P	RST_I2C_MUX3_N	I2C MUX3 reset
P4	IO_2/PLL_L_CLKOUTP/DIFFIO_RX_L27P	RST_I2C_MUX4_N	I2C MUX4 reset
U7	IO_3/DIFFIO_RX_B11N	RST_I2C_MUX5_N	I2C MUX5 reset
M9	IO_3/DIFFIO_TX_RX_B14P	RST_MAC_N	MAC reset
C2	IO_1A/ADC1IN9/DIFFIO_RX_L2N	RST_NIC1_N	I210 reset
B2	IO_8/DIFFIO_RX_T27N	RST_NIC1_PCIE_N	I210 PCIE reset
C10	IO_8/DIFFIO_RX_T17P	RST_NTM_H	Timing card reset
P3	IO_2/DIFFIO_RX_L24P	RST_PHY1_N	PHY1 reset
T3	IO_2/DIFFIO_RX_L23P	RST_PHY2_L	PHY2 reset
U11	IO_3/DIFFIO_RX_B17P	RST_SPI_BIOS_N	BISO flash reset
G1	IO_1A/ADC1IN10/DIFFIO_RX_L8P	RST_SW_BTN_N	Botton reset
M18	IO_5/DIFFIO_RX_R13N	RST_SYS_CPLD_L	BMC to CPLD reset
D2	IO_1A/ADC1IN16/DIFFIO_RX_L2P	RST_USB_BRIDGE_N	USB bridge reset
R14	IO_4/DIFFIO_TX_RX_B25N	RST_USB_SIE_N	USB SI enhancer reset
D12	IO_7/DIFFIO_RX_T3P	RST_WDT_CPLD_TO_UCD_CTRL	Watch dog to UCD
N18	IO_5/DIFFIO_RX_R13P	RSVD_CPLD_PD	Reserve
F18	IO_6/VREFB6N0	RSVD_CPLD_PU1	Reserve
P17	IO_5/VREFB5N0	RSVD_CPLD_PU2	Reserve
P18	IO_5/DIFFIO_RX_R12N	SATA_SSD_PRESENT_L	SSD present
L1	IO_1B/DIFFIO_RX_L17N	SFP_PWR_OC_GP1	Port power OC
M1	IO_2/DIFFIO_RX_L19N	SFP_PWR_OC_GP2	Port power OC
N1	IO_2/DIFFIO_RX_L21N	SFP_PWR_OC_GP3	Port power OC
N3	IO_2/DPCLK1/DIFFIO_RX_L22P	SFP_PWR_OC_GP4	Port power OC
P1	IO_2/DIFFIO_RX_L21P	SFP_PWR_OC_GP5	Port power OC
P2	IO_2/DIFFIO_RX_L24N	SFP_PWR_OC_GP6	Port power OC
R1	IO_2/VREFB2N0	SFP_PWR_OC_GP7	Port power OC
R2	IO_2	SFP_PWR_OC_GP8	Port power OC
T2	IO_2/DIFFIO_RX_L26P	SFP+_PWR_OC_GP10	Port power OC
U1	IO_2/DIFFIO_RX_L28N	SFP+_PWR_OC_GP11	Port power OC
M7	IO_2/DIFFIO_RX_L25P	SFP+_PWR_OC_GP12	Port power OC

Number	Name	Net Name	Pin Description
T1	IO_2/DIFFIO_RX_L26N	SFP+_PWR_OC_GP9	Port power OC
D7	IO_8/DIFFIO_RX_T18N	SMB_10M_DIR_SEL	SMB port 10Mhz in/out control
C9	IO_8/DIFFIO_RX_T17N	SMB_1PPS_DIR_SEL	SMB port 1pps in/out control
G17	IO_6/DIFFIO_RX_R19N	SMBUS_PECI_DIS_N	SMBUS_PECI_DIS_N
A14	IO_7/DIFFIO_RX_T5N	SSD_DEVSLP_CPLD	SSD sleep mode control
G9	IO_8/CONFIG_SEL	SYS_CPLD_BOOT_SEL	CPLD boot select
L11	IO_5/DIFFIO_RX_R8N	TPM_PP	
F2	IO_1A/ADC1IN8/DIFFIO_RX_L7P	UART_CPU_BMC_MUX_SEL	Switch console UART to BMC or CPU
G3	IO_1A/ADC1IN7/DIFFIO_RX_L7N	UART_TOD_MUX_SEL	Switch CPU UART to BMC or TOD
B11	IO_7/DIFFIO_RX_T10N	USB_GNSS_MUX_SEL	Switch CPU USB P1 to GNSS or CP2105 for TOD
B3	IO_8/DIFFIO_RX_T25N	USB_PWR_EN	USB power enable
G15	IO_6/DIFFIO_RX_R27N	USB_PWR_OC_CPU_N	USB power over current to CPU
J11	IO_6/DIFFIO_RX_R20P	USB_PWR_OC_N	USB power over current
R12	IO_4/DIFFIO_TX_RX_B23N	USB_SIE_DEV_DECTECT	USB SI enhancer detect
R13	IO_4/DIFFIO_TX_RX_B23P	USB_SIE_HS_IND	USB SI enhancer
B5	IO_8/DIFFIO_RX_T20N	USB_TOD_MUX_SEL	Switch USB P2 to CP2130 or timing card
C14	IO_7/DIFFIO_RX_T6P	WDT_CPU_TO_CPLD	CPU to CPLD watch dog
F3	ADC_VREF		Unused
C4	IO_8/CRC_ERROR/DIFFIO_RX_T22N		Unused
B8	IO_8/DEV_CLRN/DIFFIO_RX_T16N		Unused
D8	IO_8/DEV_OE/DIFFIO_RX_T18P		Unused
N13	NC0		
F7	NC1		
G7	IO_1B/DIFFIO_RX_L9N		Unused
L7	IO_2/DIFFIO_RX_L25N		Unused
R6	IO_3/DIFFIO_TX_RX_B5P		Unused
N7	IO_3/DIFFIO_TX_RX_B9N		Unused
N8	IO_3/DIFFIO_TX_RX_B9P		Unused
R8	IO_3/DIFFIO_TX_RX_B10N		Unused
R9	IO_3/DIFFIO_TX_RX_B10P		Unused
M8	IO_3/DIFFIO_TX_RX_B14N		Unused
N11	IO_4/DIFFIO_TX_RX_B18P		Unused

Number	Name	Net Name	Pin Description
N14	IO_5/DIFFIO_RX_R1P		Unused
M12	IO_5/DIFFIO_RX_R3P		Unused
K16	IO_5/DIFFIO_RX_R11N		Unused
H15	IO_6/DIFFIO_RX_R22N		Unused
H16	IO_6/DIFFIO_RX_R23N		Unused
F15	IO_6/DIFFIO_RX_R27P		Unused
F16	IO_6/DIFFIO_RX_R28N		Unused
G16	IO_6/DIFFIO_RX_R28P		Unused
E16	IO_6/DIFFIO_RX_R29P		Unused
G12	IO_6/DIFFIO_RX_R31N		Unused
G11	IO_6/DIFFIO_RX_R31P		Unused
D13	IO_7/DIFFIO_RX_T3N		Unused
F12	IO_7/DIFFIO_RX_T8N		Unused
C12	IO_7/DIFFIO_RX_T9P		Unused
D9	IO_8/DIFFIO_RX_T12N		Unused
D10	IO_8/DIFFIO_RX_T12P		Unused
F10	IO_8/DIFFIO_RX_T14P		Unused
C8	IO_8/DIFFIO_RX_T21P		Unused
D5	IO_8/DIFFIO_RX_T26N		Unused
D6	IO_8/DIFFIO_RX_T26P		Unused
M6	VCCA_1	N20535516	VCCA
F14	VCCA_2	N20535516	VCCA
F6	VCCA_3_1	N20535516	VCCA
F4	VCCA_3_2	N20535516	VCCA
P13	VCCA_4	N20535516	VCCA
L9	VCC_ONE_1	P3V3_STB	VCC_ONE
K10	VCC_ONE_2	P3V3_STB	VCC_ONE
J9	VCC_ONE_3	P3V3_STB	VCC_ONE
H10	VCC_ONE_4	P3V3_STB	VCC_ONE
F13	VCC_ONE_5	P3V3_STB	VCC_ONE
C3	VCC_ONE_6	P3V3_STB	VCC_ONE
N6	VCC_ONE_7	P3V3_STB	VCC_ONE
H5	VCCIO1A_1	P3V3_STB	VCCIO
G5	VCCIO1A_2	P3V3_STB	VCCIO
K5	VCCIO1B_1	P3V3_STB	VCCIO
J5	VCCIO1B_2	P3V3_STB	VCCIO
M5	VCCIO2_1	P3V3_STB	VCCIO

Number	Name	Net Name	Pin Description
L6	VCCIO2_2	P3V3_STB	VCCIO
L5	VCCIO2_3	P3V3_STB	VCCIO
P9	VCCIO3_1	P3V3_STB	VCCIO
P8	VCCIO3_2	P3V3_STB	VCCIO
P7	VCCIO3_3	P3V3_STB	VCCIO
N9	VCCIO3_4	P3V3_STB	VCCIO
P12	VCCIO4_1	P3V3_STB	VCCIO
P11	VCCIO4_2	P3V3_STB	VCCIO
M13	VCCIO5_1	P3V3_STB	VCCIO
L14	VCCIO5_2	P3V3_STB	VCCIO
L13	VCCIO5_3	P3V3_STB	VCCIO
K14	VCCIO5_4	P3V3_STB	VCCIO
J14	VCCIO6_1	P3V3_STB	VCCIO
J13	VCCIO6_2	P3V3_STB	VCCIO
H13	VCCIO6_3	P3V3_STB	VCCIO
G14	VCCIO6_4	P3V3_STB	VCCIO
G13	VCCIO6_5	P3V3_STB	VCCIO
E12	VCCIO7_1	P3V3_STB	VCCIO
E11	VCCIO7_2	P3V3_STB	VCCIO
D11	VCCIO7_3	P3V3_STB	VCCIO
F9	VCCIO8_1	P3V3_STB	VCCIO
E9	VCCIO8_2	P3V3_STB	VCCIO
E8	VCCIO8_3	P3V3_STB	VCCIO
E7	VCCIO8_4	P3V3_STB	VCCIO
A1	GND_1	GND	GND
A18	GND_2	GND	GND
B10	GND_3	GND	GND
B15	GND_4	GND	GND
B6	GND_5	GND	GND
D3	GND_6	GND	GND
E10	GND_7	GND	GND
E13	GND_8	GND	GND
E6	GND_9	GND	GND
F17	GND_10	GND	GND
F8	GND_11	GND	GND
G2	GND_12	GND	GND
G4	GND_13	GND	GND

Number	Name	Net Name	Pin Description
H14	GND_14	GND	GND
J10	GND_15	GND	GND
J17	GND_16	GND	GND
K13	GND_17	GND	GND
K6	GND_18	GND	GND
K9	GND_19	GND	GND
L4	GND_20	GND	GND
M14	GND_21	GND	GND
N10	GND_22	GND	GND
N12	GND_23	GND	GND
N17	GND_24	GND	GND
N2	GND_25	GND	GND
N5	GND_26	GND	GND
R7	GND_27	GND	GND
U10	GND_28	GND	GND
U14	GND_29	GND	GND
U4	GND_30	GND	GND
V1	GND_31	GND	GND
V18	GND_32	GND	GND

3.3 *MB CPLD Register Mapping*

Switch board CPLD can be accessed through LPC with based address 0x700.

Offset	Register Name	Mark
0x00	Board information 0	Board information
0x01	Board information 1	
0x02	CPLD version	CPLD information
0x03	CPLD boot up image	
0x04	Boot select	
0x05	Clock & timing status	Clock & Timing
0x06	Clock & timing control	
0x07	System Status	
0x08	Power Status	Power
0x09	Power & system control	
0x0A	ROV status	
0x0B	ROV control	
0x0C	I210 control	
0x0D	GNSS status	
0x0E	GNSS control	
0x0F	TPM control	
0x10	UART control	
0x11	USB status	
0x12	USB control	
0x13	I2C MUX select	
0x14	FAN Present	
0x15	SFP over current	
0x16	SFP+ over current	
0x17	PSU Status	
0x18	Clock & PTP reset	Reset
0x19	System reset	
0x1A	ETH Reset	
0x1B	I2C MUX reset	
0x1C	USB SIE reset	

Offset	Register Name	Mark
0x1D	Clock & PTP interrupt	
0x1E	Clock & PTP interrupt mask	
0x1F	PSU interrupt	Interrupt
0x20	System reset	
0x21	HWM interrupt	
0x22	HWM interrupt mask	
0x23	Thermal interrupt	
0x24	Thermal interrupt mask	
0x25	VCORE interrupt	
0x26	VCORE interrupt mask	
0x27	FAN Interrupt	
0x28	FAN Interrupt mask	
0x29	ETH interrupt	
0x2A	ETH interrupt mask	
0x2B	Port interrupt	
0x2C	Port interrupt mask	
0x2D	CPU NMI interrupt	
0x2E	CPU NMI interrupt mask	
0x2F	Intrude interrupt	
0x30	Intrude interrupt mask	
0x31	Interrup output status	
0x32	Interrup output mask	
0x33	Watch dog status	Watch Dog
0x34	Watch dog control	
0x35	LED clear	LED
0x36	Front panel LED control	
0x37	LED Blink	

3.4 MB CPLD Register Description

Board information 0				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x00	7	CPLD_BUILD_ID1	0	
	6	CPLD_BUILD_ID0	0	
	5	CPLD_HW_REV_ID1	0	
	4	CPLD_HW_REV_ID0	0	
	3	CPLD_SKU_ID3	0	
	2	CPLD_SKU_ID2	0	
	1	CPLD_SKU_ID1	1	
	0	CPLD_SKU_ID0	1	

Board information 1				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x01	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4		0	
	3	CPLD_REV_ID3	0	
	2	CPLD_REV_ID2	0	
	1	CPLD_REV_ID1	0	
	0	CPLD_REV_ID0	0	

CPLD version				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x02	7		0	
	6		0	
	5		0	
	4		0	
	3		0	

	2		0	
	1		0	
	0		0	

CPLD boot up image				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x03	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	Reserved	x	
	3	Reserved	x	
	2	Reserved	x	
	1	Reserved	x	
	0		0	0: CPLD boot up from image 0 1: CPLD boot up from image 1

Boot select				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x04	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	Reserved	x	
	3	Reserved	x	
	2	PHY2_SERBOOT		0: PHY2 init by MDIO 1: PHY2 init by flash
	1	BIOS_BOOT_SEL1		00:BIOS0 on COME module , BIOS1 on Carrier board , Default boot up from COME 01:BIOS0 on COME module , BIOS1 on Carrier board , Default boot up from Carrier 10:BIOS0/BIOS1 on COME module , boot up from carrier firmware hub 11:BIOS0/BIOS1 on COME module , boot up from COME BIOS
	0	BIOS_BOOT_SEL0		

Clock & timing status

Offset	Bit	Pin / Function	Default Value	Description
0x05	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	Reserved	x	
	3	PHY1_SYNCE_RCVD_LOCK	0	0: PHY 1 SYNCE is not locked 1: PHY 1 SYNCE is locked
	2	LOCK_MAC_SYNCE_RCVD1	0	0: MAC SYNCE is not locked 1: MAC SYNCE is locked
	1	MAC_MCUPLL_LOCK	0	0: MAC MCU PLL is not locked 1: MAC MCU PLL is locked
	0	MAC_COREPLL_LOCK	0	0: MAC core PLL is not locked 1: MAC core PLL is locked

Clock & timing control				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x06	7	P3V3_EN_BROADSYNC	1	0: Disable BROADSYNC power 1: Enable BROADSYNC power
	6	PTP_1PPS_BITS_MUX_SEL	0	0: BITS 1PPS input from T1E1 1.544M 1: BITS 1PPS input from SMB 1PPS
	5	SMB_10M_DIR_SEL	0	0: SMB input 10Mhz 1: SMB output 10Mhz
	4	SMB_1PPS_DIR_SEL	0	0: SMB input 1PPS 1: SMB output 1PPS
	3	PTP_UART_RS422_DIR_CNTRL	0	0: UART TOD to CPU (active when UART_TOD_MUX_SEL = 1) 1: UART CPU to TOD (active when UART_TOD_MUX_SEL = 1)
	2	PTP_TOD_RS422_DIR_CNTRL	0	0: UART_TOD_RS422_TXD active 1: UART_TOD_RS422_RXD active
	1	PTP_10M_RS422_DIR_CNTRL	0	0: CLK_10M_TOD_IN active 1: CLK_DPLL_10M_TOD_OUT active
	0	PTP_1PPS_RS422_DIR_CNTRL	0	0: CLK_1PPS_TOD_IN active 1: CLK_1PPS_TOD_OUT active

System Status

Offset	Bit	Pin / Function	Default Value	Description
0x07	7	SATA_SSD_PRESENT_L	0	0: SSD is present 1: SSD is absent
	6	NTM_PRSNT_L	0	0: Timing card is present 1: Timing card is absent
	5	BMC_PRSNT_L	0	0: Timing card is present 1: Timing card is absent
	4	CPU_THRMTRIP_CPLD_L	1	0: CPU Thermaltrip assert 1: CPU Thermaltrip de-assert
	3	CPU_SUS_STAT_L		0: 1:
	2	CPU_SUS_S5_L	0	0: CPU is in S5 state 1: CPU is not in S5 state
	1	CPU_BOOT_DONE_TO_CPLD	0	0: CPU booting is not done 1: CPU boot is done
	0	CPU_PLT_RST_L	0	0: CPU platform reset assert 1: CPU platform reset de-assert

Power Status				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x08	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	CPU_BATLOW_L		0: CPU battery power voltage is low 1: CPU batteriy power voltage is normal
	3	P3V3_BMC_PG		0: P3V3_BMC power is not ready 1: P3V3_BMC power is ready
	2	PWRGD_BMC_TO_SYS		0: BMC board power is not ready 1: BMC board power is ready
	1	CPU_PWRGD_TO_CPLD		0: CPU board power is not ready 1: CPU board power is ready
	0	PWROK_SYS_DC		0: Main board power is not ready 1: Main board power is ready

Power & system control				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**

0x09	7	Reserved	x	
	6	Reserved	x	
	5	I2C_HWM_CNTRL	x	
	4	SSD_DEVSLP_CPLD	1	0: SSD is in normal mode 1: SSD is in sleep mode
	3	PWRBTN_CPLD_TO_CPU_N	1	0: Pull PWRBTN_CPLD_TO_CPU_N low for 20 ms .Reset to defual when CPU power good de-assert. 1: Normal mode.
	2	PWREN_CPLD_TO_CPU	1	0: Pull CPU PWROK low 1: Pull CPU PWROK high
	1	PWREN_SYS_DC_CPU_L	1	0: Disable main board DC(Except for stanby power) 1: Enable main board DC(Except for stanby power)
	0	PWREN_SYS_P12V_CPU_L	1	0: Disable 12v 1: Enable 12v

ROV status				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x0A	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	Reserved	x	
	3	Reserved	x	
	2	MAC_VCORE_ROV2	0	
	1	MAC_VCORE_ROV1	0	
	0	MAC_VCORE_ROV0	0	

ROV control				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x0B	7			
	6			
	5			
	4			

	3			
	2			
	1			
	0			

I210 control				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x0C	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	Reserved	x	
	3	Reserved	x	
	2	Reserved	x	
	1	Reserved	x	
	0	NIC1_DEV_OFF_N	1	0: I210 is in device disable mode 1: I210 is in normal mode

GNSS status				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x0D	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	Reserved	x	
	3	Reserved	x	
	2	GNSS_ANT_ON	1	0:GNSS antenna is off 1:GNSS antenna is on
	1	GNSS_ANT_OPEN	0	0:GNSS antenna is connected 1:GNSS antenna is open
	0	GNSS_ANT_SHORT_N	0	0:GNSS antenna is short 1:GNSS antenna is connected

GNSS control				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x0E	7	Reserved	x	
	6	Reserved	x	

	5	Reserved	x	
	4	Reserved	x	
	3	Reserved	x	
	2	Reserved	x	
	1	Reserved	x	
	0	GNSS_ANT_PWREN	1	0:GNSS antenna power disable 1:GNSS antenna power enable

TPM control				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x0F	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	Reserved	x	
	3	Reserved	x	
	2	Reserved	x	
	1	Reserved	x	
	0	TPM_PP		

UART control				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x10	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	Reserved	x	
	3	Reserved	x	
	2	Reserved	x	
	1	UART_TOD_MUX_SEL	1	0: CPU UART connect to BMC 1: CPU UART connect to TOD port
	0	UART_CPU_BMC_MUX_SEL	0	0: Console UART connect to CPU 1: Console UART connect to BMC

USB status				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**

0x11	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	Reserved	x	
	3	USB_PWR_OC_CPU_N	1	0: USB port is over current(Output to CPU) 1: USB port is not over current(Output to CPU)
	2	USB_PWR_OC_N	1	0: USB port is over current(Input from USB port) 1: USB port is not over current(Input from USB port)
	1	USB_SIE_HS_IND		
	0	USB_SIE_DEV_DECTECT		

USB control				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x12	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	Reserved	x	
	3	USB_PWR_EN	1	0: Disable USB port power 1: Enable USB port power
	2	USB_TOD_MUX_SEL	1	0: USB2_PCH_P2 connect to BITS 1: USB2_PCH_P2 connect to timing card
	1	USB_GNSS_MUX_SEL	1	0: USB2_PCH_P1 connect to GNSS 1: USB2_PCH_P2 connect to CP2105
	0	BMC_USB_MUX_SEL		0: USB port connect to CPU USB2_PCH_P0 1: USB port connect to BMC

I2C MUX select				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x13	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	I2C0_HWM_MUX_SEL		0: I2C0_HWM connect to I2C1_BMC 1: I2C0_HWM connect to CPU I2C
	3	I2C0_PSU_MUX_SEL		0: I2C0_PSU connect to I2C2_BMC

I2C MUX select				
				1: I2C0_PSU connect to CPU I2C
	2	I2C_MANF_MUX_SEL		0: I2C0_MANF connect to I2C4_BMC 1: I2C0_MANF connect to CPU I2C
	1	I2C_CPLD_MUX_EN		0: I2C0_CPLD connect to I2C3_BMC 1: I2C0_CPLD connect to CPU I2C
	0	SMBUS_PECI_DIS_N		0: Disable CPU legacy SMB to BMC PECI connection 1: Enable CPU legacy SMB to BMC PECI connection

FAN Present				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x14	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	Reserved	x	
	3	HWM_FAN4_PRSNT_N		0: FAN4 is present 1: FAN4 is absent
	2	HWM_FAN3_PRSNT_N		0: FAN3 is present 1: FAN3 is absent
	1	HWM_FAN2_PRSNT_N		0: FAN2 is present 1: FAN2 is absent
	0	HWM_FAN_PRSNT_N		0: All FAN is present 1: All FAN is absent

SFP over current				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x15	7	SFP_PWR_OC_GP8		0: Port 18/19 power switch is over current 1: Port 18/19 power switch is not over current
	6	SFP_PWR_OC_GP7		0: Port 16/17 power switch is over current 1: Port 16/17 power switch is not over current
	5	SFP_PWR_OC_GP6		0: Port 14/15 power switch is over current 1: Port 14/15 power switch is not over current
	4	SFP_PWR_OC_GP5		0: Port 12/13 power switch is over current

				1: Port 12/13 power switch is not over current
	3	SFP_PWR_OC_GP4		0: Port 10/11 power switch is over current 1: Port 10/11 power switch is not over current
	2	SFP_PWR_OC_GP3		0: Port 8/9 power switch is over current 1: Port 8/9 power switch is not over current
	1	SFP_PWR_OC_GP2		0: Port 6/7 power switch is over current 1: Port 6/7 power switch is not over current
	0	SFP_PWR_OC_GP1		0: Port 4/5 power switch is over current 1: Port 4/5 power switch is not over current

SFP+ over current				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x16	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	Reserved	x	
	3	SFP+_PWR_OC_GP12		0: Port 26/27 power switch is over current 1: Port 26/27 power switch is not over current
	2	SFP+_PWR_OC_GP11		0: Port 24/25 power switch is over current 1: Port 24/25 power switch is not over current
	1	SFP+_PWR_OC_GP10		0: Port 22/23 power switch is over current 1: Port 22/23 power switch is not over current
	0	SFP+_PWR_OC_GP9		0: Port 20/21 power switch is over current 1: Port 20/21 power switch is not over current

PSU Status				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x17	7	Reserved	x	
	6	Reserved	x	
	5	PSU2_VOUT_PWROK	1	0: PSU2 VOUT power is not ok 1: PSU2 VOUT power ok
	4	PSU1_VOUT_PWROK	1	0: PSU1 VOUT power is not ok 1: PSU1 VOUT power ok
	3	PSU2_VIN_PWROK	1	0: PSU2 VIN power is not ok 1: PSU2 VIN power ok

	2	PSU1_VIN_PWROK	1	0: PSU1 VIN power is not ok 1: PSU1 VIN power ok
	1	PSU2_PRSNT_N	0	0: PSU2 is present 1: PSU2 is absent
	0	PSU1_PRSNT_N	0	0: PSU1 is present 1: PSU1 is absent

Clock & PTP reset				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x18	7	Reserved	x	
	6	RST_BITS_N	1	0: BITS reset assert 1: BITS reset de-assert
	5	RST_CP2104_TOD_N	1	0: CP2105 reset assert 1: CP2105 reset de-assert
	4	RST_USB_BRIDGE_N	1	0: USB bridge CP2130 reset assert 1: USB bridge CP2130 reset de-assert
	3	RST_GNSS_N	1	0: GNSS reset assert 1: GNSS reset de-assert
	2	RST_NTM_H	1	0: Timing card reset assert 1: Timing card reset de-assert
	1	RST_CJA_N	1	0: SI5344 reset assert 1: SI5344 reset de-assert
	0	RST_CLK_GEN_N	1	0: Clock generator ZL30262 reset assert 1: Clock generator ZL30262 reset de-assert

System reset				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x19	7	Reserved	x	
	6	Reserved	x	
	5	RST_SPI_BIOS_N	1	0: Main board BIOS flash reset assert 1: Main board BIOS flash reset de-assert
	4	RST_BMC_LPC_N	1	0: BMC LPC reset assert 1: BMC LPC reset de-assert
	3	RST_BMC_PCIE_N	1	0: BMC PCIE reset assert 1: BMC PCIE reset de-assert
	2	RST_CPLD_TO_BMC_SYS_L	1	0: BMC system reset assert 1: BMC system reset de-assert

	1	RST_CPLD_TO_CPU_N	1	0: CPU system reset assert 1: CPU system reset de-assert
	0	Global reset	1	0: Global reset assert 1: Global reset de-assert

ETH Reset				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x1A	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	RST_NIC1_PCIE_N	1	0: I210 PCIE reset assert 1: I210 PCIE reset de-assert
	3	RST_NIC1_N	1	0: I210 reset assert 1: I210 reset de-assert
	2	RST_PHY2_L	1	0: PHY2 reset assert 1: PHY2 reset de-assert
	1	RST_PHY1_N	1	0: PHY1 reset assert 1: PHY1 reset de-assert
	0	RST_MAC_N	1	0: MAC reset assert 1: MAC reset de-assert

I2C MUX reset				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x1B	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	RST_I2C_MUX5_N	1	0: I2C MUX5 reset assert 1: I2C MUX5 reset de-assert
	3	RST_I2C_MUX4_N	1	0: I2C MUX4 reset assert 1: I2C MUX4 reset de-assert
	2	RST_I2C_MUX3_N	1	0: I2C MUX3 reset assert 1: I2C MUX3 reset de-assert
	1	RST_I2C_MUX2_N	1	0: I2C MUX2 reset assert 1: I2C MUX2 reset de-assert
	0	RST_I2C_MUX0_N	1	0: I2C MUX0 reset assert 1: I2C MUX0 reset de-assert

USB SIE reset				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x1C	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	Reserved	x	
	3	Reserved	x	
	2	Reserved	x	
	1	Reserved	x	
	0	RST_USB_SIE_N	1	0: USB port SI enhancer reset assert 1: USB port SI enhancer reset de-assert

Clock & PTP interrupt				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x1d	7	Reserved	x	
	6	INT_BITS_N	1	0: BITS interrupt assert 1: BITS interrupt de-assert
	5	INT_CJA_LOL_N	1	0: SI5344 LOL interrupt assert 1: BSI5344 LOL interrupt de-assert
	4	INT_CJA_INTR_N	1	0: SI5344 interrupt assert 1: BSI5344 interrupt de-assert
	3	INT1_GNSS_N	1	0: GNSS interrupt assert 1: GNSS interrupt de-assert
	2	INT_DPLL_SYNC_L	1	0: DPLL SYNC interrupt assert 1: DPLL SYNC interrupt de-assert
	1	INT_DPLL_1588_L	1	0: DPLL 1588 interrupt assert 1: DPLL 1588 interrupt de-assert
	0	INT_NTM_L	1	0: Timing card interrupt assert 1: Timing card interrupt de-assert

Clock & PTP interrupt mask				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x1E	7		x	
	6		0	0: Disable BITS interrupt mask

				1: Enable BITS interrupt mask
	5		0	0: Disable SI5344 LOL interrupt mask 1: Enable BSI5344 LOL interrupt mask
	4		0	0: Disable SI5344 interrupt mask 1: Enable BSI5344 interrupt mask
	3		0	0: Disable GNSS interrupt mask 1: Enable GNSS interrupt mask
	2		0	0: Disable DPLL SYNC interrupt mask 1: Enable DPLL SYNC interrupt mask
	1		0	0: Disable DPLL 1588 interrupt mask 1: Enable DPLL 1588 interrupt mask
	0		0	0: Disable timing card interrupt mask 1: Enable timing card interrupt mask

PSU interrupt				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x1F	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	Reserved	x	
	3	Reserved	x	
	2	Reserved	x	
	1	INT_PSU2_N	1	0: PSU2 interrupt assert 1: PSU2 interrupt de-assert
	0	INT_PSU1_N	1	0: PSU1 interrupt assert 1: PSU1 interrupt de-assert

PSU interrupt mask				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x20	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	Reserved	x	
	3	Reserved	x	
	2	Reserved	x	
	1		0	0: Disable PSU2 interrupt mask

				1: Enable PSU2 interrupt mask
	0		0	0: Disable PSU1 interrupt mask 1: Enable PSU1 interrupt mask

HWM interrupt				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x21	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	Reserved	x	
	3	Reserved	x	
	2	Reserved	x	
	1	INT_HWM_ALERT_N	1	0: HWM ALERT assert 1: HWM ALERT de-assert
	0	INT_HWM_NMI_N	1	0: HWM NMI interrupt assert 1: HWM NMI interrupt de-assert

HWM interrupt mask				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x22	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	Reserved	x	
	3	Reserved	x	
	2	Reserved	x	
	1		0	0: Disable HWM interrupt mask 1: Enable HWM interrupt mask
	0		0	0: Disable HWM NMI interrupt mask 1: Enable HWM NMI interrupt mask

Thermal interrupt				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x23	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	

	4	Reserved	x	
	3	Reserved	x	
	2	INT_TSEN_ALRT_N	1	0: TSEN ALRT assert 1: TSEN ALRT de-assert
	1	INT_THRM_CHIP_N	1	0: THRM_CHIP interrupt assert 1: THRM_CHIP interrupt de-assert
	0	INT_TSEN_NMI_N	1	0: TSEN NMI interrupt assert 1: TSEN NMI interrupt de-assert

Thermal interrupt mask				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x24	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	Reserved	x	
	3	Reserved	x	
	2		0	0: Disable TSEN ALRT interrupt mask 1: Enable TSEN ALRT interrupt mask
	1		0	0: Disable THRM_CHIP interrupt mask 1: Enable THRM_CHIP interrupt mask
	0		0	0: Disable TSEN NMI interrupt mask 1: Enable TSEN NMI interrupt mask

VCORE interrupt				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x25	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	Reserved	x	
	3	Reserved	x	
	2	Reserved	x	
	1	INT_VCORE_ALRT_N	1	0: VCORE ALRT assert 1: VCORE ALRT de-assert
	0	INT_VCORE_VR_FAULT_N	1	0: VCORE VR_FAULT interrupt assert 1: VCORE VR_FAULT interrupt de-assert

VCORE interrupt mask				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x26	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	Reserved	x	
	3	Reserved	x	
	2	Reserved	x	
	1		0	0: Disable VCORE ALRT mask 1: Enable VCORE ALRT mask
	0		0	0: Disable VCORE VR_FAULT interrupt mask 1: Enable VCORE VR_FAULT interrupt mask

FAN Interrupt				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x27	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	Reserved	x	
	3	INT_FAN4_N	1	0: FAN4 interrupt assert 1: FAN4 interrupt de-assert
	2	INT_FAN3_N	1	0: FAN3 interrupt assert 1: FAN3 interrupt de-assert
	1	INT_FAN2_N	1	0: FAN2 interrupt assert 1: FAN2 interrupt de-assert
	0	INT_FAN_CARD_N	1	0: FAN card interrupt assert 1: FAN card interrupt de-assert

FAN Interrupt mask				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x28	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	Reserved	x	
	3		0	0: Disable FAN4 interrupt mask

				1: Enable FAN4 interrupt mask
	2		0	0: Disable FAN3 interrupt mask 1: Enable FAN3 interrupt mask
	1		0	0: Disable FAN2 interrupt mask 1: Enable FAN2 interrupt mask
	0		0	0: Disable FAN card interrupt mask 1: Enable FAN card interrupt mask

ETH interrupt				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x29	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	Reserved	x	
	3	I2C_NIC_ARLT_N	1	0: I210 ARLT assert 1: I210 ARLT de-assert
	2	PHY2_INT_N	1	0: PHY2 interrupt assert 1: PHY2 interrupt de-assert
	1	INT_PHY1_N	1	0: PHY1 interrupt assert 1: PHY1 interrupt de-assert
	0	INT_MAC_N	1	0: MAC interrupt assert 1: MAC interrupt de-assert

ETH interrupt mask				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x2A	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	Reserved	x	
	3		0	0: Disable I210 ARLT mask 1: Enable I210 ARLT mask
	2		0	0: Disable PHY2 interrupt mask 1: Enable PHY2 interrupt mask
	1		0	0: Disable PHY1 interrupt mask 1: Enable PHY1 interrupt mask
	0		0	0: Disable MAC interrupt mask

				1: Enable MAC interrupt mask

Port interrupt				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x2B	7	Reserved	x	
	6	Reserved	x	
	5	INT_SFP+_LOS_N1	1	0: IO expander SFP LOS 1 interrupt assert 1: IO expander SFP LOS 1 interrupt de-assert
	4	INT_SFP+_LOS_N0	1	0: IO expander SFP LOS 0 interrupt assert 1: IO expander SFP LOS 0 interrupt de-assert
	3	INT_SFP+_FLT_N1	1	0: IO expander SFP FLT 1 interrupt assert 1: IO expander SFP FLT 1 interrupt de-assert
	2	INT_SFP+_FLT_N0	1	0: IO expander GNSS interrupt assert 1: IO expander GNSS interrupt de-assert
	1	INT_SFP+_ABS_N1	1	0: IO expander SFP ABS 1interrupt assert 1: IO expander SFP ABS 1 interrupt de-assert
	0	INT_SFP+_ABS_N0	1	0: IO expander SFP ABS 0 interrupt assert 1: IO expander SFP ABS 0 interrupt de-assert

Port interrupt mask				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x2C	7	Reserved	x	
	6	Reserved	x	
	5		0	0: Disable IO expander SFP LOS 1 interrupt mask 1: Enable IO expander SFP LOS 1 interrupt mask
	4		0	0: Disable IO expander SFP LOS 0 interrupt mask 1: Enable IO expander SFP LOS 0 interrupt mask
	3		0	0: Disable IO expander SFP FLT 1 interrupt mask 1: Enable IO expander SFP FLT 1 interrupt mask
	2		0	0: Disable IO expander SFP FLT 0 interrupt mask 1: Enable IO expander SFP FLT 0 interrupt mask

	1		0	0: Disable IO expander SFP ABS 1 interrupt mask 1: Enable IO expander SFP ABS 1 interrupt mask
	0		0	0: Disable IO expander SFP ABS 0 interrupt mask 1: Enable IO expander SFP ABS 0 interrupt mask

CPU NMI interrupt				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x2D	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	Reserved	x	
	3	Reserved	x	
	2	Reserved	x	
	1	Reserved	x	
	0	NMI_CPU_TO_CPLD_L	1	0: CPU NMI interrupt assert 1: CPU NMI interrupt de-assert

CPU NMI interrupt mask				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x2E	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	Reserved	x	
	3	Reserved	x	
	2	Reserved	x	
	1	Reserved	x	
	0		0	0: Disable CPU NMI interrupt mask 1: Enable CPU NMI interrupt mask

Intrude interrupt				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**

0x2F	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	Reserved	x	
	3	Reserved	x	
	2	Reserved	x	
	1	Reserved	x	
	0	INT_INTRUDER_CPLD_N	1	0: INTRUDER interrupt assert 1: INTRUDER interrupt de-assert

Intrude interrupt mask				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x30	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	Reserved	x	
	3	Reserved	x	
	2	Reserved	x	
	1	Reserved	x	
	0		0	0: Disable INTRUDER interrupt mask 1: Enable INTRUDER interrupt mask

Interrup output status				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x31	7	Reserved	x	
	6	I2C_CPLD_ALRT_N	1	0: To BMC I2C ALRT assert 1: To BMC I2C ALRT de-assert
	5	NMI_SYS_TO_BMC_N	1	0: To BMC NMI interrupt assert 1: To BMC NMI interrupt de-assert
	4	INT_THRM_CPLD_TO_CPU_L	1	0: To CPU THRM interrupt assert 1: To CPU THRM interrupt de-assert
	3	INT_ETH_TO_CPU_N	1	0: To CPU ETH interrupt assert 1: To CPU ETH interrupt de-assert
	2	INT_PTP_TO_CPU_N	1	0: To CPU PTP interrupt assert 1: To CPU PTP interrupt de-assert
	1	NMI_CPLD_TO_CPU_N	1	0: To CPU NMI interrupt assert

				1: To CPU NMI interrupt de-assert
	0	INT_CPLD_TO_CPU_N	1	0: To CPU I2C ALERT assert 1: To CPU I2C ALERT de-assert

Interrup output mask				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x32	7	Reserved	x	
	6		0	0: Disable to BMC I2C ALRt mask 1: Enable to BMC I2C ALRt mask
	5		0	0: Disable to BMC NMI interrupt mask 1: Enable to BMC NMI interrupt mask
	4		0	0: Disable to CPU tHRM interrupt mask 1: Enable to CPU tHRM interrupt mask
	3		0	0: Disable to CPU EtH interrupt mask 1: Enable to CPU EtH interrupt mask
	2		0	0: Disable to CPU PtP interrupt mask 1: Enable to CPU PtP interrupt mask
	1		0	0: Disable to CPU NMI interrupt mask 1: Enable to CPU NMI interrupt mask
	0		0	0: Disable to CPU I2C ALERt mask 1: Enable to CPU I2C ALERt mask

Watch dog status				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x33	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	Reserved	x	
	3	Reserved	x	
	2	RST_BMC_WDT1		
	1	RST_BMC_WDT2		
	0	WDT_CPU_TO_CPLD		

Watch dog control

Offset	Bit	Pin / Function	Default Value	Description
0x34	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	Reserved	x	
	3	Reserved	x	
	2	Reserved	x	
	1	Reserved	x	
	0	RST_WDT_CPLD_TO_UCD_CTRL		

LED clear				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x35	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	Reserved	x	
	3	Reserved	x	
	2	LED_ETH_STAT_CLR_N	x	0：Clear port LED 1：Normal state
	1	LED_FAN_CLR_N	1	0：Clear FAN LED 1：Normal state
	0	LED_SYS_STAT_CLR_N	1	0：Clear Front Panel LED 1：Normal state

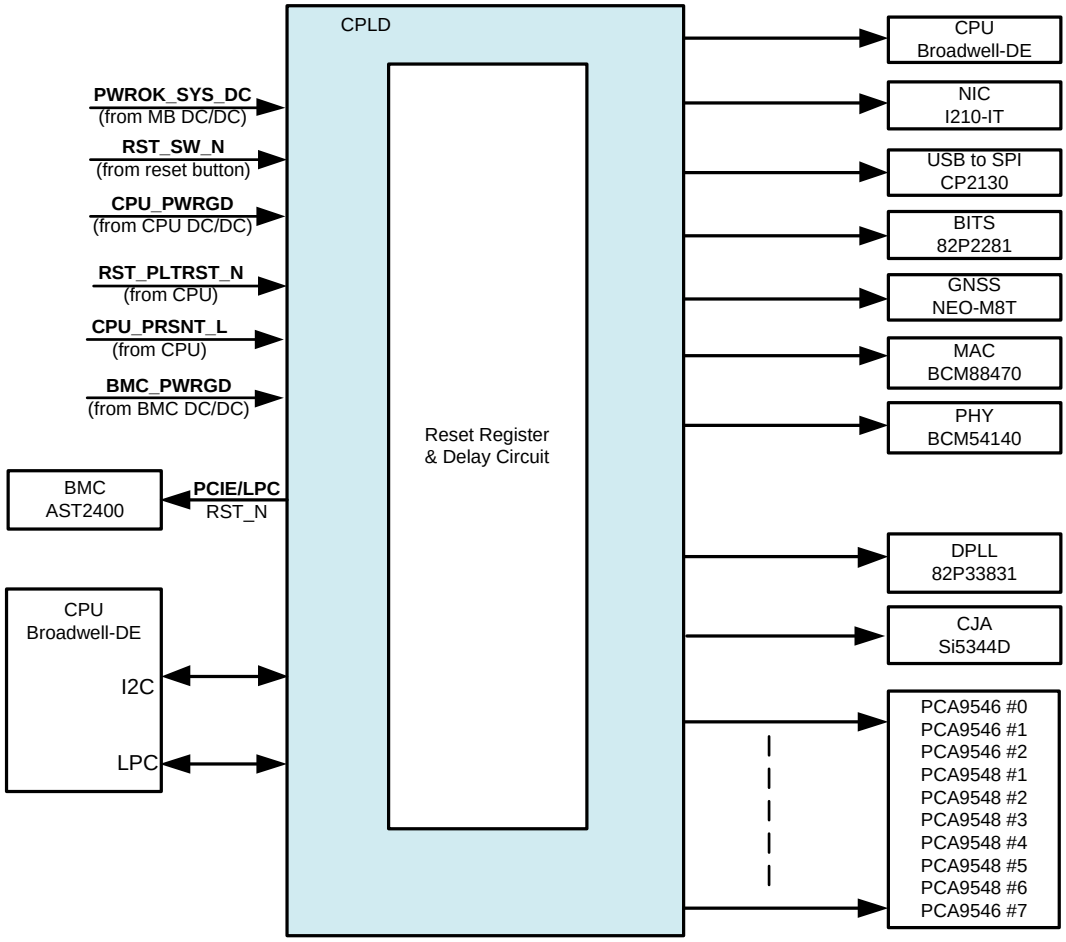
Front panel LED control				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x36	7	Reserved	x	
	6	Reserved	x	
	5	System Status LED color	1	0：Yellow 1：Green
	4	System Status LED On/Off	1	0：Off 1：On
	3	GNSS Status LED color	1	0：Yellow 1：Green

	2	GNSS Status LED On/Off	1	0：Off 1：On
	1	SYNC Status LED color	1	0：Yellow 1：Green
	0	SYNC Status LED On/Off	1	0：Off 1：On

LED Blink				
Offset	**Bit**	**Pin / Function**	**Default Value**	**Description**
0x37	7	Reserved	x	
	6	Reserved	x	
	5	Reserved	x	
	4	Reserved	x	
	3	Reserved	x	
	2	System Status LED Blinking Status	0	0：Stable 1：Blinking
	1	GNSS Status LED Blinking Status	0	0：Stable 1：Blinking
	0	SYNC Status LED Blinking Status	0	0：Stable 1：Blinking

4 Interrupt

4.1 *Reset Control*



4.2 Hardware reset button

CPLD make the different reaction when the time to push reset button is different.

- Pushing button for less than 5s, CPLD will reset the whole system, except BMC.
- Pushing button for more than 5s, CPLD has no response.

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4.3 *CPLD Interrupt Management*

There are 5 interrupt signals to X86 CPU GPIO1, GPIO6, GPIO7, GPIO12, GPIO15 used for interrupt purpose, these GPIO pins should be configured as interrupt input and handle these events according to pre-defined priority. Any one of NMI, CHIP, PTP, SFP interrupts will generate an I2C alert event to CPU SMBus alert pin.

Receiving the 'Load Factory Default Interrupt', CPU should proceed system reboot and BIOS/ONIE/NOS images/pass words recovery to factory default.

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4.3.1 Hardware Non-Maskable Interrupt

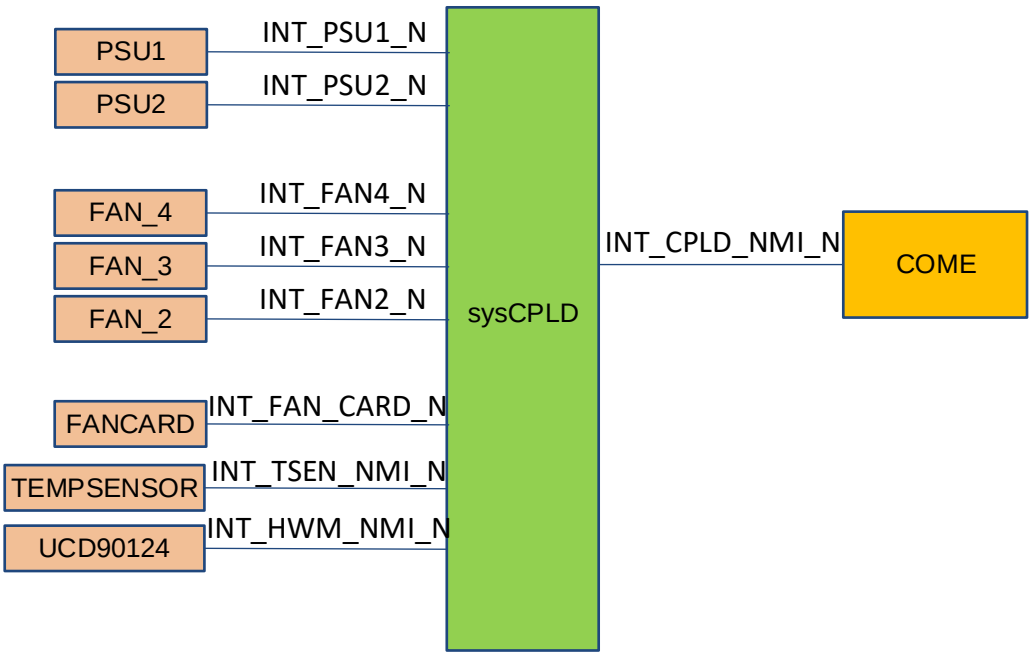


Figure 4-1 NMI Interrupt

4.3.2 Ethernet MAC/PHY Status Interrupt

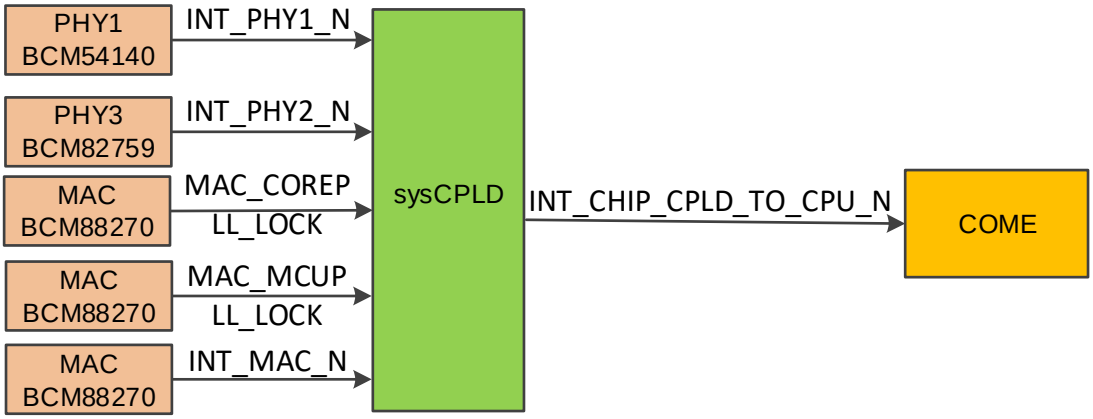


Figure 4-2 MAC &PHY Interrupt

4.3.3 SyncE and PTP Status Interrupt

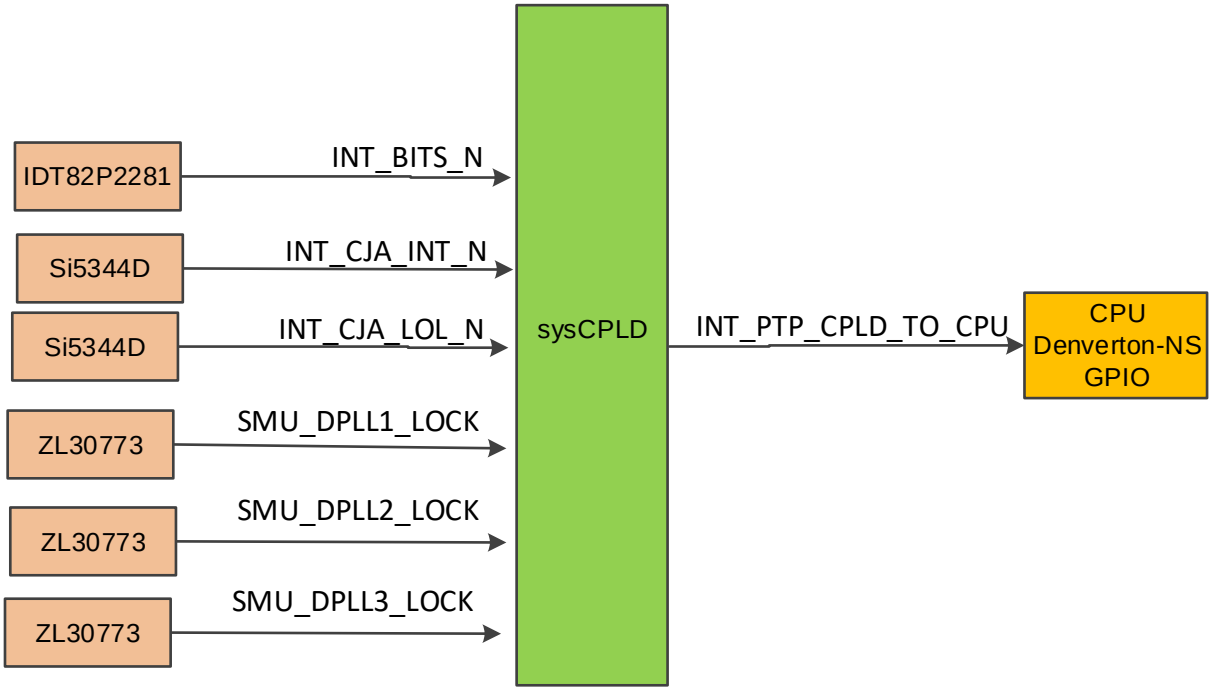


Figure 4-3 SyncE &PTP Interrupt

4.3.4 SFP/SFP+ Port Status Interrupt

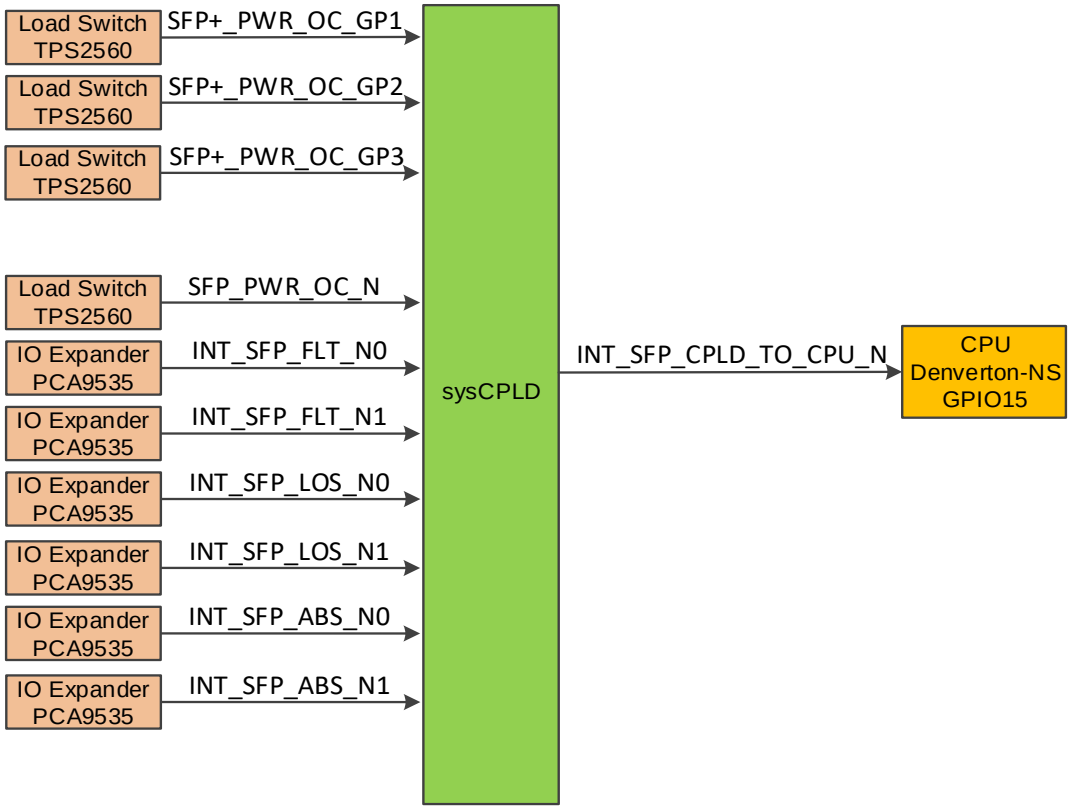


Figure 4-4 SFP Interrupt

4.3.5 CPLD Alarm Interrupt

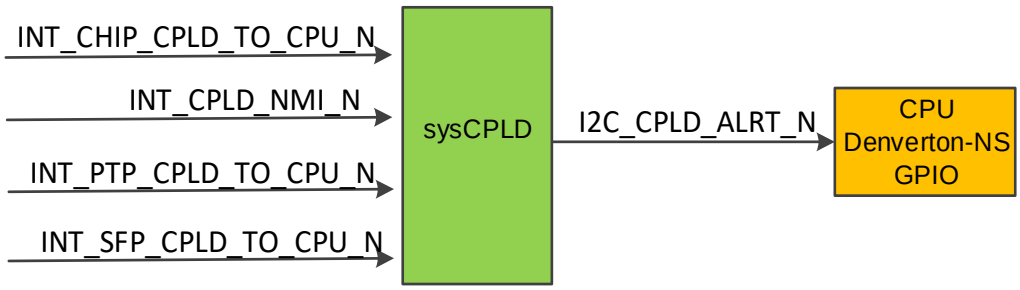


Figure 4-5 CPLD I2C Alarm Interrupt

5 LED

The front panel system status LED are placed on Main board. The bit stream of serial LED interface is shown as below:

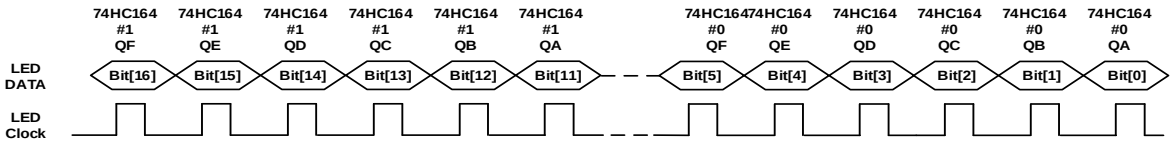


Figure 5-1 Bit stream of Front Panel LED interface

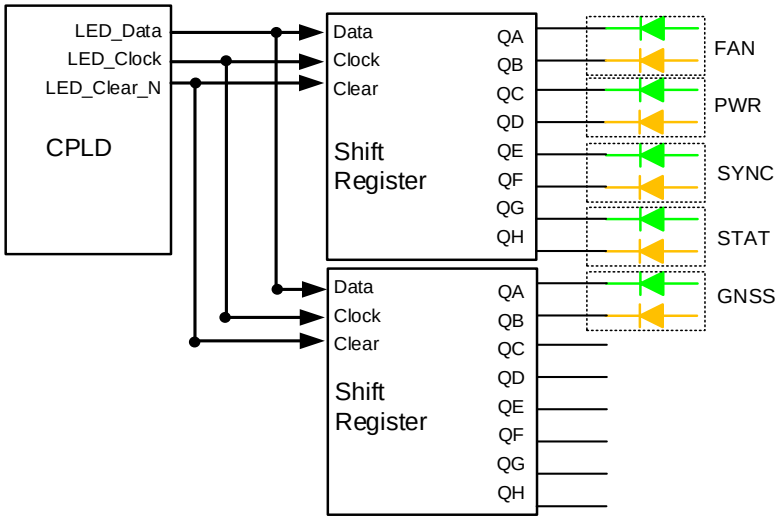


Figure 5-2 Front Panel LED Diagram

LED Function/State	*Meaning*	*Comment*
PWR (Green/Yellow): controlled by CPLD LED Interface Bit [0:1]		
OFF	No power or in shutdown mode.	Bit [0]=1; Bit [1]=1
Solid Green	System power good & BMC is present & BMC power good	Bit [0]=0; Bit [1]=1
Blinking Green (1Hz on / 1Hz off)	System power good & BMC is present but BMC power fail	Bit [0]=0; Bit [1]=**B**
Solid Yellow	System power good & BMC is absent	Bit [0]=1; Bit [1]=0
Blinking Yellow (0.5Hz)	System power fail	Bit [0]=**B**; Bit [1]=0
FAN (Green/Yellow): controlled by CPLD LED Interface Bit [2:3]		
OFF	Reserved	Bit [0]=1; Bit [1]=1
Solid Green	All FAN modules work well	Bit [0]=0; Bit [1]=1
Blinking Green	Reserved	Bit [0]=0; Bit [1]=**B**
Solid Yellow	Reserved	Bit [0]=1; Bit [1]=0
Blinking Yellow	One or more FAN module(s) fail or no FAN module present	Bit [0]=**B**; Bit [1]=0
STAT (Green/Yellow): controlled by CPLD LED Interface Bit [4:5]		
OFF	System (X86 & BMC) no boot	Bit [2]=1; Bit [3]=1
Solid Green	System boot complete (NOS) **Note: need NOS to integrate this feature	Bit [2]=0; Bit [3]=1

LED Function/State	*Meaning*	*Comment*
Blinking Green	System is booting	Bit [2]=**B**; Bit [3]=1
Solid Yellow	System boot complete (DIAG OS)	Bit [2]=1; Bit [3]=0
Blinking Yellow	Reserved	Bit [0]=**B**; Bit [1]=0
GNSS (Green/Yellow): controlled by CPLD LED Interface Bit [8:9]		
OFF	GNSS is not configured. **Note: need NOS to integrate this feature	Bit [8]=1; Bit [9]=1
Solid Green	GNSS is in normal state. Self-survey is complete. **Note: need NOS to integrate this feature	Bit [8]=0; Bit [9]=1
Blinking Green	GNSS is in learning state. Self-survey is not completed. **Note: need NOS to integrate this feature	Bit [8]= **B**; Bit [9]=1
Solid Yellow	Power up. GNSS is not tracking any satellite. **Note: need NOS to integrate this feature	Bit [8]=1; Bit [9]=0
Blinking Yellow	GNSS antenna is short to ground. **Note: need NOS to integrate this feature	Bit [8]= **B**; Bit [9]=1
SYNC (Green/Yellow): controlled by CPLD LED Interface Bit [10:11]		
OFF	System timing synchronization is disabled or in free-run mode. **Note: need NOS to integrate this feature	Bit [10]=1; Bit [11]=1
Solid Green	System timing core(1588 and SyncE) is synchronized to external timing source (ex: GNSS, 1PPS, PTP, BITS, etc) **Note: need NOS to integrate this feature	Bit [10]=0; Bit [11]=1
Blinking Green	System is synchronized in SyncE mode. **Note: need NOS to integrate this feature	Bit [10]= **B**; Bit [11]=1
Solid Yellow	System timing core is in acquiring state or holdover mode. **Note: need NOS to integrated this feature	Bit [10]=1; Bit [11]=0
Blinking Yellow	System timing synchronization fail. **Note: need NOS to integrated this feature	Bit [10]=1; Bit [11]= **B**
Note : **B**= Blinking, interleaved bit value with 1 and 0		